In the Specification

Please replace paragraph [0001] with the following:

[0001] This present application relates to commonly-assigned U.S. Patent Application Serial No.[[_____]] 10/614,495, filed July 7, 2003, now U.S. Patent No. 6,987,419, issued on Jan. 17, 2006, Attorney Docket No18054 (1110-03).

Please DELETE paragraph [0011].

Please DELETE paragraph [0012].

Please replace paragraph [0013] with the following:

[0013] Figures ~~5~~ 3(a)-~~5~~ 3(i) are graphs showing a frequency versus decibel (dB) response for the switch circuit of Figure 2 in various states.

Please replace paragraph [0014] with the following:

[0014] Figure ~~6~~ 4 shows a schematic diagram of a conventional Gilbert Cell.

Please replace paragraph [0016] with the following:

[0016] One conventional technique for multiplying two signals together in an IC is through the use of a Gilbert Cell. As is well known in the art, a Gilbert Cell is typically implemented as a cross-coupled differential amplifier. Figure [[6]] 4 shows an exemplary Gilbert Cell 100 which includes a first differential amplifier pair 110 (including transistors 111, 112), and a second differential amplifier pair 120 (including transistors 121, 122). The collectors of transistors 111 and 121 are coupled to each other and to pin "5" of the Gilbert Cell 100. Similarly, the collectors of transistors 112 and 122 are coupled to each other and to pin "6" of the Gilbert Cell 100. Further, the bases of transistors 111 and 122 are coupled to each other and to pin "8" of the Gilbert Cell 100, and the bases of transistors 112 and 121 are coupled to each other and to pin "7" of the Gilbert Cell. Finally, the emitters of the transistors 111, 112 of the first differential amplifier pair 110 are coupled

to the collector of a first bias transistor 130, and the emitters of the transistors 121, 122 of the second differential amplifier pair 120 are coupled to the collector of a second bias transistor 140. In operation, a differential AC bias voltage applied to the bases of the first and second bias transistors 130, 140 (through pins "1" and "4" of the Gilbert Cell) controls the amplitude of an input radiofrequency (RF) signal applied across pins "6" and "7" of the Gilbert Cell. As shown and described in the following figures, the present inventors propose various modifications of a Gilbert Cell so that it may be used as a DPST switch, as opposed to its traditional use as an amplifier.

Please replace paragraph [0021] with the following:

[0021] In accordance with the first exemplary embodiment of the present invention, a portion of the network of transistor switches 208 is laid out similarly to the above-described Gilbert Cell. In particular, the network includes bias transistors 240, 240' , 241, and 241' (corresponding to bias transistors 130, 140 of the Gilbert Cell shown in Figure [[14]] 4), interior transistors 245, 246 (corresponding to transistors 112, 121 of the Gilbert Cell shown in Figure [[14]] 4), and exterior transistors 247, 248 (corresponding to transistors 111, 122 of the Gilbert Cell shown in Figure [[14]] 4). However, instead of interior transistors 245, 246 having their bases coupled together they are decoupled. Further, additional transistors 250-257 are provided around the 'modified' Gilbert Cell. For ease of illustration, not all of the biasing circuitry for each of the transistors 240, 240', 241, 241', 245-248 and 250-257 is shown in Figure 2(b).

Please replace paragraph [0027] with the following:

[0027] Figure 3 shows the switch circuit 200 of Figure 2 implemented monolithically. Figure 4 is an enlarged view of a portion of the monolithically-implemented switch circuit 200 showing the input ports 201, 202, and the output port 203 in greater detail. It should be noted that the switch circuit 200 of Figure 2 may also be implemented monolithically.

Please replace paragraph [0028] with the following:

[0028] Figures [[5]] 3(a)-[[5]] 3(i) are graphs showing a frequency in GigaHertz (GHz) versus decibel (dB) response for the switch circuit 200 of Figure 2. In particular, Figures [[5]] 3(a), (e) and (i) show input impedance matching curves for input ports 201 (Port 1), 202 (Port 2) and output port 203 (Port 3), respectively. The remaining figures show isolation curves for the switch circuit 200 as between different ports (e.g., Figure [[5]] 3(b) shows an isolation curve between one of the input ports (Port 2) and another of the input ports (Port 1). As will be recognized by those skilled in the art, the isolation between the ports 201-203 of the switch circuit 200 is relatively uniform across the operational frequency range. As will be noted by those of ordinary skill in the art, the switch circuit 200 is always matched (i.e., the return loss of each port 201-203 stays constant irrespective of the switch's state).